Kiet Vu

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Education

Purdue University, B.Sc. in Computer Engineering *Expected May 2029*
West Lafayette, IN GPA: 3.93/4.0
Expected Coursework: ASIC Design Laboratory, Microprocessor Systems and Interfacing, Computer Design and Prototyping, Semiconductor Devices

Projects

Open-source Contributor | *Accel-Sim/GPGPU-Sim GPU Simulator* June 2026 – Present

- Inferred that Nsight Compute counts L2 writes allocated without a DRAM fetch as hits; added a matching counter **(merged upstream)**, closing a **0% vs. 100%** sim/HW gap on a streaming-write microbenchmark and raising Rodinia write-hit correlation **0.88 → 0.999**
- Found that NVIDIA's L2 write counters include local-memory (register-spill) traffic the correlator ignored; fixing it raised ISPASS-2009 correlation **-0.06 → 0.9999**
- Wrote a microbenchmark showing hardware merges L1→L2 writes (**4× traffic gap** at equal L1 hit rate); prototyped a merge buffer (**19.10% → 2.33%** mean error, 32 apps) but withheld it after the same benchmark showed the buffer can't be the real mechanism
- Fixed a PTX-parser bug restoring PTX-mode simulation on CUDA 11+ (merged upstream) and root-caused a SIGSEGV in the FP64 pipeline model

Jane Street ASIC Reverse-Engineering Puzzle | *Python, Yosys, LibreLane, SAT* Aug. 2026 – Sep. 2026

- Reverse-engineered an 11×11 Star Battle validator and rebuilt it RTL→GDS with 0 DRC/LVS violations; selected as a **Jane Street favorite solution**
- Recovered a **738-gate** sky130 netlist from raw GDSII with a from-scratch parser and union-find connectivity extractor; validated **84/84** nets against a reference design and bit-exact over 312 cycles of the vendor waveform
- Proved the rebuild equivalent to the original for every input board using SAT-based bounded model checking (2M variables, 5.4M clauses)

32-bit RISC-V Pipelined Processor | *SystemVerilog, Computer Architecture* Feb. 2026 – Mar. 2026

- Designed a 5-stage pipelined RV32I processor supporting the complete base integer instruction set, achieving **100% architectural compliance** via the RISCOF framework by co-simulating against Spike reference model
- Synthesized the core targeting the Sky130 node via LibreLane to generate a verified GDSII layout; used high-speed standard cells to achieve a peak frequency of **95.2 MHz (0.551 mm^2)** with clean STA and LVS signoffs

KV-PIMple: PIM-aware KV-allocation for LLM Decode | *HBM, PIM, AI Systems* Sep. 2026

- Showed that vLLM's paged KV allocation breaks the DRAM row alignment PIM all-bank attention depends on; designed a region allocator derived from HBM geometry, raising row-hit rate from **0.77 to 0.96** and effective bandwidth **2.3×** in my model (**1.6×** on AttAcc's cycle-level PIM controller)
- Built a continuous-batching decode simulator around a port of vLLM v0.2.7's block allocator; evaluated steady, long-context, prefix-sharing, and speculative-decoding workloads, and cross-validated row-hit against Ramulator 2 **(within 0.0023)**

Experience

Undergraduate Researcher, Purdue SoCET GPU Team Aug. 2026 – Present

- Led a team of 3 designing the Ethernet RX datapath for a fixed-function GPU on FPGA; implemented the frame detector, address parser, and CRC-32 in SystemVerilog, verified in simulation
- Defined the host-to-GPU command protocol over raw Ethernet, specifying payload formats for register writes and vertex streaming

Undergraduate Researcher, Purdue EPICS HDR Aug. 2025 – May 2026

- Refactored multiple legacy data source modules to standardized abstract base class architecture, implementing consistent data pipeline, improving maintainability and code reusability

Extracurricular Activities

Technical Member, Purdue RoboMaster Aug. 2025 – May 2026

- Engineered PCBs for a rechargeable armor plate, fluorescent projectile charger, and an audio visualizer circuit

Technical Skills

Languages: Verilog/SystemVerilog, C/C++, Tcl, CUDA, PTX/SASS, MATLAB, Python
Computer Architecture: GPU architecture, RISC-V, I/O Interface, Ethernet, AMBA, FPGA
Software: LibreLane Toolchains, Yosys, Surfer, Linux, GitHub, EasyEDA, Altium, VS Code, Nsight Tools